# Innovative Integration Solutions for SiP Packages Using Fan-Out Wafer Level eWLB Technology

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**Abstract**

Fan-Out Wafer Level Packaging (FOWLP) has been established as one of the most versatile packaging technologies in the recent past and already accounts for a market value of over 1 billion USD due to its unique advantages. The technology combines high performance, increased functionality with a high potential for heterogeneous integration and reduced overall form factor as well as cost effectiveness. The increasing complexities in achieving a higher degree of performance, bandwidth and better power efficiency in various markets are pushing the boundaries of emerging packaging technologies to smaller form factor packaging designs with finer line/width spacing as well as improved thermal/electrical performance and the integration of System-in-Package (SiP) or 3D capabilities.

SiP technology has been evolving through utilization of various package technology building blocks to serve the market needs with respect to miniaturization, higher integration, and smaller form factor as cited above, with the added benefits of lower cost and faster time to market as compared to silicon (Si) level integration, which is commonly called system-on-chip or SoC. As such, SiP incorporates flip chip (FC), wire bond (WB), and fan-out wafer-level packaging (FOWLP) as its technology building blocks and serves various end applications ranging from radio frequency (RF), power amplifiers (PA), Micro-Electro-Mechanical-Systems (MEMS) and Sensors, and connectivity, to more advanced application processors (AP), and other logic devices such as graphics processing units (GPUs)/central processing units (CPUs). FOWLP, also referred to as advanced embedded Wafer Level Ball Grid Array (eWLB) technology, provides a versatile platform for the semiconductor industry's technology evolution from single or multi-die 2D package designs to 2.5D interposers and 3D SiP configurations.

This paper presents developments in SiP applications with eWLB/Fan-out WLP technology, integration of various functional blocks such as wire bonding, Package-on-Package (PoP), 2.5D, 3D, smaller form factor, embedded passives, multiple redistribution layer routing and z-height reduction. Test vehicles have been designed and fabricated to demonstrate and characterize these low profile and integrated packaging solutions for mobile products including Internet of Things (IoT)/wearable electronics (WE), MEMS and sensors. Finer line/width spacing of 2/2mm with multiple redistribution layers (RDL) are fabricated and implemented on the eWLB platform to enable higher interconnect density and signal routing. Assembly process details, component level reliability, board level reliability and characterization results for eWLB SiP will be discussed.

## I. Introduction

The semiconductor industry is constantly faced with complex integration challenges as consumers want their electronics to be smaller, faster and higher performance with more and more functionality packed into a single device. The demand for such requirements have driven

many new trends and innovations in advanced packaging technology.

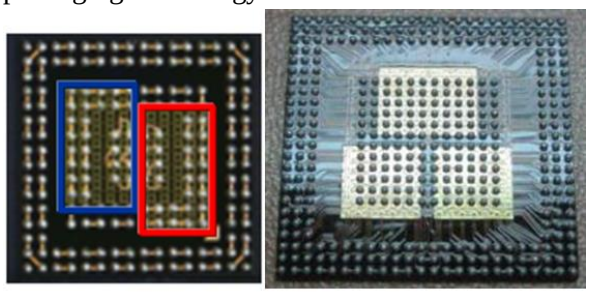

Figure 1a. SiP in eWLB

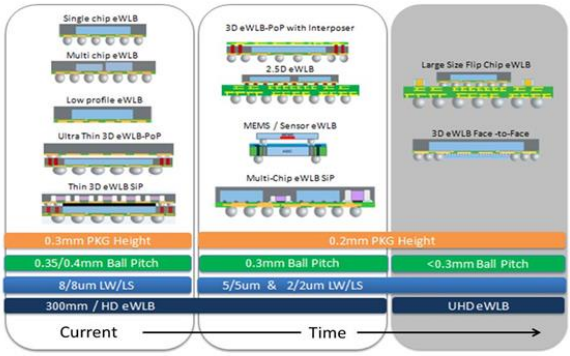


Figure 1b. SiP in eWLB trend

One of the solutions is System-in-Package (SiP). System-in-Package is a functional electronic system or sub-system that includes two or more heterogeneous semiconductor die (often from different technology nodes optimized for their individual functionalities), usually with passive components. The physical form of the SiP is a module, and depending on the end application, the module could include a logic chip, memory, integrated passive devices (IPD), RF filters, sensors, heat sinks, antennas, connectors and/or power chip in packaged or bare die form. . This paradigm shift from chip scaling to system level scaling will continue to reinvent microelectronics packaging and help sustain Moore's Law [7]. The challenge of the semiconductor industry is to develop a disruptive packaging technology capable of rapidly achieving these goals.

To meet the above challenges, embedded Wafer Level Ball Grid Array (eWLB) is a technology platform that offers additional space for routing higher input/output (I/O) on top of the silicon chip area which is not possible in conventional wafer level packaging or wafer level bump. Figure 1 shows the eWLB packages and package evolution to 2.5D and 3D SiP. eWLB also offers comparatively better electrical, thermal and reliability performance at a reduced cost with the possibility to address additional advanced technology Si nodes with low k-dielectrics in a multi-die or 3D eWLB package.

**Embedded Wafer Level BGA (eWLB) Technology**

Fan-Out eWLB is an innovative approach designed to provide flexibility to accommodate an unlimited number of interconnects between the package and the application board for maximum connection density, finer line/width spacing, improved electrical and thermal performance and small package dimensions. A Wafer Level Chip Scale Package (WLCSP) structure, also known as Fan-In Wafer Level Packaging, is compared to a Fan-out eWLB structure in Figure 2.


Figure 2. Fan In WLP vs. Fan Out WLP

Unlike conventional WLCSP, the first step in eWLB manufacturing is to thin and singulate the incoming silicon wafer. Following singulation, an artificial wafer (or panel) is then created by embedding the diced silicon chips onto a blank metal carrier. The main reconstitution steps shown in Figure 3 include:

1) The reconstitution process starts by laminating an adhesive foil onto a carrier ( artificial wafer/panel )
2) Singulated die are placed faced down with a pick and place tool

3) Die are encapsulated with molding compound
4) After curing the mold compound, the carrier and foil are removed, resulting in a reconstituted wafer. The molding compound will only surround exposed die surfaces.

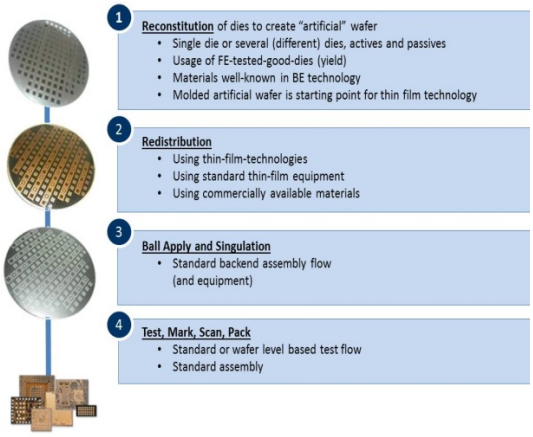


**Figure 3. Process Flow for eWLB**

## II. Various Applications of eWLB in SiP

**Mobile RF, PMIC, Connectivity**

eWLB/FOWLP in a SiP configuration is a growing trend for advanced application processors, MEMS and sensors in IoT/WE as a way to cost effectively achieve advanced silicon die partitioning for increased performance and integration in a reduced form factor [7].

Figure 4 shows a 3D eWLB SiP/module with several discrete components in the top package and is pre-stacked on the bottom eWLB-PoP to form a 3D SiP/module with a thin package profile of 1.0mm total height. Twelve discretes, including inductors and multilayer ceramic capacitors (MLCCs) were removed from the motherboard and relocated in the top package for a reduction in space on the motherboard.

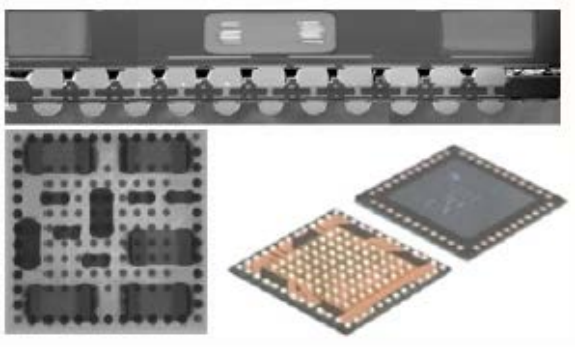

**Figure 4. 3D SiP eWLB-PoP with discretes in interposer on top package**

The discretes are also more power efficient when they are close to the device, significantly improving the overall electrical performance as well as providing a power saving advantage.

Functional test samples were prepared with power management integrated circuit (PMIC) as shown in Figure 4. The SiP has a 6mm x 6mm body size with a 4mm x 4mm Si die and 12 discretes on the top. This eWLB SiP demonstrated more power efficiency performance compared to other embedded package technology and is representative of a significantly smaller package solution [5,7].

**MEMS/Sensor eWLB**

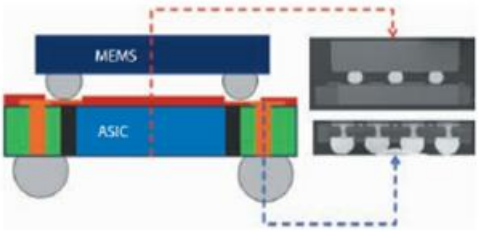


**Figure 5. 3D eWLB for MEMS/Sensor Devices [2]**

Figure 5 illustrates an eWLB sensor which has been miniaturized from the original side-by-side land grid array (LGA) package. It has a 3D vertical interconnection and multi-die stacking. It provides over 20% footprint reduction and less than 1mm thickness with a lower cost high

volume manufacturing (HVM) solution. The smaller body sizes (5mm/side or less) are typically a good fit for sensor devices such as health monitoring and environmental sensors.

Since sensor devices typically require at least a two chip solution (example application specific integrated circuit and MEMS/Sensing silicon), advanced eWLB/FOWLP stack up solutions can enable a very small pitch LGA and ball grid array ( BGA) eWLB PoP footprint at a competitive cost vs. the incumbent wire bond solutions.

The package architecture enables routing on both sides of the package by embedding a direct via across the top to pad side of the package. The top MEMS device is bumped through standard lead frame wafer processing, singulated and assembled by pick and place tooling and reflow on the application specific integrated circuit (ASIC) in the eWLB bottom package. This assembly will eliminate the need for die attach material, assembly wires, protective glob-top and also the typical metal cap or molded package with access cavity thus removing the typical laminate or leadframe for routing. Consequently, 3D eWLB SiP offers a much smaller footprint, simplified bill of material and is assembled with a cost competitive panel level manufacturing process [7,10].

**Integrated Passives in eWLB-SiP**

In mobile applications for GSM/WCDMA /EDGE technologies, many functional blocks such as Power Amplifier (PA), Baluns, transceiver, filters, etc., play a key role in the performance of the module. Even though a PA made from gallium arsenide (GaAs) is widely used due to its good electrical and thermal properties, they are quite expensive. In an RF circuit, a power amplifier has an impedance matching circuit consisting of capacitors and inductors which consume a significant portion of the die size and can be potentially be replaced by an IPD and successfully used for RF modules/SiP in PA impedance matching and coupling circuits [8].

For this PA module, a multi-chip eWLB has been developed with a PA and IPD integrated side-by-side.

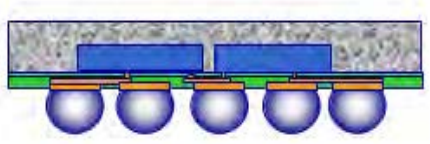

**Figure 6. Side view of PA and IPD in SIP**

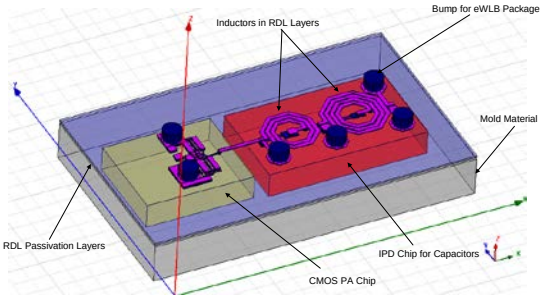


**Figure 7. Illustration of a PA die and silicon IPD die embedded in mold substrate**

Figure 6 and 7 illustrates an eWLB package, which includes a PA chip and an IPD chip. The IPD die mainly serves as an impedance matching network for the PA.

In this multi-die eWLB package the connection from the RDL to the PA chip is made through the via connecting the RDL layer and the top metal layer in the PA chip. The connection between the RDL and the IPD chip is made through via connecting the RDL layer and the top thick metal layer in the IPD. There are three different substrates in this package; a complementary metal-oxide-semiconductor (CMOS) substrate, IPD substrate and mold compound substrate are shown in Figure 8. The passivation redistribution layers are fabricated through a standard thin film process, plating in wafer fabrication process, thus forming a multi-

die eWLB package after standard backend processes.

### 2/2um Line Width and Spacing (LW/LS) with 3-Layer RDL [2]

High I/O with fine pitch area array continues to be one of the greatest challenges in wafer level packaging. Redistribution layer (RDL) allows signal and supply I/O's to be redistributed to a footprint larger than the chip footprint in eWLB. Required line widths and spacing of 2/2um for eWLB applications support the bump pitch of less than 40um. Finer line width and spacing are critical for multi die design and routing flexibility.

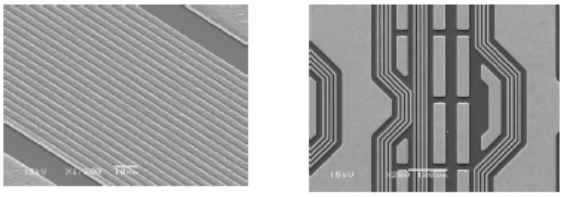

**Figure 8. SEM of 2/2um LW/LS RDL with coarser RDL LW/LS**

Figure 8 shows 2/2um (LW/LS) alongside coarser LW/LS in eWLB/FOWLP. Scanning Electron Microscope (SEM) images show uniform and well defined micro structure. Copper (Cu) RDL thickness and critical dimensions (CD) are also well controlled with verified process robustness using current HVM equipment and process flow [7].

## III. Reliability Performance

### Electrical Performance of 3D eWLB PoP/SiP vs. fcPoP

The RLC parasitic values for eWLB-PoP/SiP and fcPoP were extracted by computer simulation using commercial 2D electromagnetic field solver. The S-parameter of each package was extracted by using ANSOFT HFSS. Simulated results are compared with RLC parasitic values and S parameters The simulation modeling design was carried out with functional devices to investigate package level performance in real applications. In 3D simulation works, a few critical pins were selected and evaluated, such as clock, VDD as well as Data pins [7].

| Net | Inductance, L (nH) | | | Resistance, R (mΩ) | | |
|---|---|---|---|---|---|---|
| | fcPoP | eWLB -PoP | Δ (%) | fcPoP | eWLB -PoP | Δ (%) |
| 1 | 1.77 | 0.43 | -76% | 240 | 67 | -72% |
| 2 | 2.03 | 0.24 | -88% | 308 | 42 | -86% |
| 3 | 1.51 | 0.57 | -62% | 348 | 112 | -68% |
| 4 | 1.08 | 0.25 | -77% | 268 | 66 | -75% |

**Table 1. Electrical Parasitic Values of RL of eWLB-PoP/SiP vs. fcPoP @ 1GHz**

For signal integrity study with specific data pins, eWLB showed more than 10dB better cross-talk than flip chip due to its thinner CuRDL and overall shorter interconnection length as shown in Figure 9. In addition, smooth CuRDL surface of wafer fab process contributed significantly with less conductance loss.

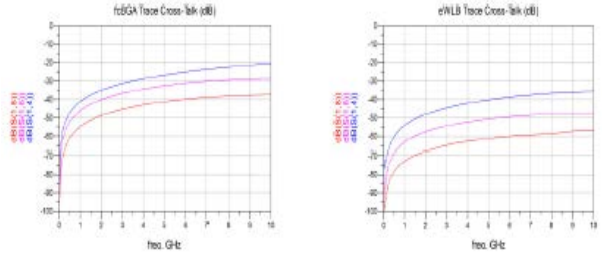

**Figure 9. The cross-talk with frequency of signal routing of (a) flip chip (b) eWLB**

### Board Level Reliability of 3D eWLB-PoP/SiP

For board level reliability tests, eWLB-PoP (stacked with top package) was pre-stacked with top memory and mounted on the printed circuit board (PCB). For PoP assembly, a 0.4mm body thickness Fine Pitch Ball Grid Array (FBGA) top package was assembled separately with standard wirebonding process and finally pre-

stacked on eWLB-PoP bottom package. The total eWLB-PoP stacked package height was less than 0.8mm in height after surface mount technology (SMT) manufacturing on the PCB. Those samples were tested in JEDEC Temperature Cycling on Board (TCoB) and drop test reliability conditions.

| Tests | Conditions | Status |
|---|---|---|
| TCoB | JEDEC JESD22-A103 -40°C to 125°C | Pass |
| Drop Test | JEDEC JESD22-B111 1500G | Pass |

**Table 2. Board Level Reliability Test Results of 3D eWLB PoP/SiP**

Table 2 shows 3D eWLB-PoP board level reliability of JEDEC TCoB and drop test results of test vehicle 1 and 2 (Table 1 and Figure 10). The first TCoB failure was after 1000 cycles. Drop reliability performance was robust and showed no failure after 300 drops. These test results show the robustness of board level reliability of 3D eWLB-PoP [7].

## III. Conclusions

eWLB technology is addressing a wide range of packaging concerns, from packaging cost to test. In parallel, there are physical constraints such as its foot print and height. Other parameters that were considered during the development phase included I/O density, a particular challenge for small ships with a high pin count as need to accommodate SiP approaches, thermal issues related to power consumption and the device's electrical performance (including electrical parasitic and operating frequency).

Advanced low profile and integrated 3D eWLB-PoP/SiP was developed using eWLB (FOWLP Technology. 3D reliability conditions board level reliability tests of pre-stacked PoP were ran through JEDEC standard conditions and showed robust reliability in TCoB and drop tests. electrical characterizations were also performed with functional devices and signal integrity simulation and showed enhanced performance of 3D eWLB-PoP compared to conventional flip chip Package-on-package (fcPoP) devices. Integrated Passives with PA modules in eWLB-SiP show impedence improvement and passed Board Level Reliability (BLR) requirements.

Advanced eWLB SiP technology provides a smaller form factor and increased performance value, proving to be a new SiP packaging platform than can expand its application range to various types of emerging mobile, Internet of Things, Wearable Electronic applications, MEMS/Sensors or Automotive applications [9].

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